IP Core

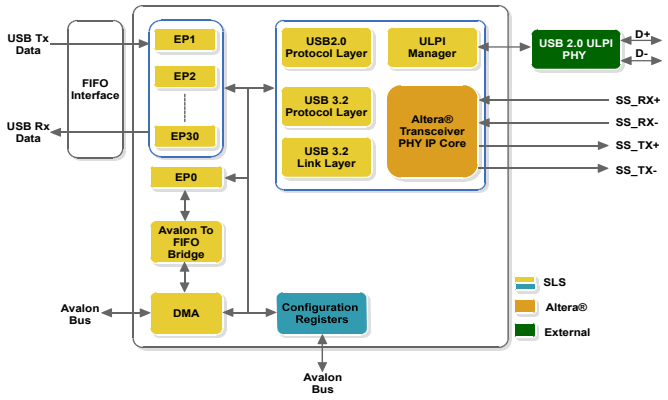
USB 20Gbps Device - Software Enumeration, FIFO Interface

A one-stop solution for USB 3.2 and USB 2.0

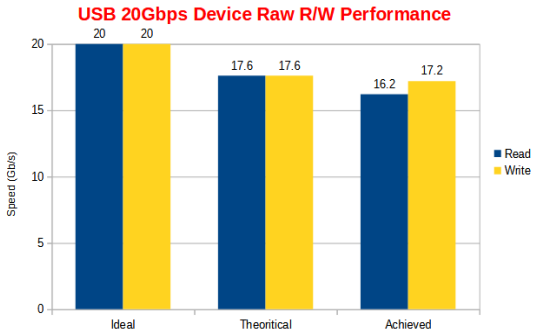
Leveraging the benefits of USB 10Gbps and 5Gbps device controller, USB 20Gbps is designed using the Altera® FPGA built-in transceiver. It is a one-stop solution for all USB requirements ranging from USB 3.2 to USB 2.0. It supports SuperSpeed+(SSP x2/x1), SuperSpeed(SS), High Speed (HS) and Full Speed (FS) communication modes. The Core architecture allows to use minimal pins from FPGA for USB 3.2 interface with better stability. It provides USB 2.0 backward compatibility using an external USB 2.0 ULPI PHY.

It has been designed to provide simplicity and flexibility along with ***highest throughput i.e. >16 Gbps***. Avalon interface allows to manage the control transfer using software, provides flexibility, while FIFO interface allows to transfer the data over non-control endpoint ensuring highest throughput.

Architecture



Performance Results



Notes:
(1).Check out Device R/W Performance Video at https://youtu.be/kbDIc7HsUvk
(2).Support for USB 20Gbps on Agilex 7 is coming soon !!!

Features

- USB 3.2 Specific Features
  - Supports USB 20Gbps, USB 10Gbps and USB 5Gbps
  - Uses Altera® Transceiver as a PHY layer and thus eliminates need for external PHY for USB 3.2
- USB 2.0 Specific Features
  - Supports High Speed (HS) and Full Speed (FS) modes
  - Provides ULPI interface to interact with external USB 2.0 PHY
- Ease of Use
  - Ready to use component for Quartus Platform designer.
  - Simple FIFO interface to transfer data over non-control endpoint
- Flexibility
  - Capable to support up to 31 endpoints (1 default control endpoint, 15 IN endpoints and 15 OUT endpoints)
  - Allows to select number of buffers per endpoint based on the requirement

Application

- Imaging Device
- Storage Device
- Machine Vision
- Data Centers

Licensing

- **OpenCore Plus Evaluation**: 1 month evaluation license at no cost
- **Full**: Project based Perpetual License
- **Maintenance**: 20% of License fees from next year to continue technical support and getting updates for IP Core

Implementation Results

Device	Resources	Memory Bits	Memory Blocks
Cyclone 10 (up to Gen 2x2 20Gbps interface)	~29184 ALM	~825152	~141 M20K
Arria 10 (up to Gen 2x2 20Gbps interface)	~28912 ALM	~825152	~141 M20K
Stratix 10 (up to Gen 2x2 20Gbps interface)	~31188 ALM	~818768	~129 M20K
Agilex 7 (up to Gen 2 10Gbps Interface)	~14870 ALM	~598944	~91 M20K
Stratix 10 (up to Gen 2 10Gbps Interface)	~14788 ALM	~596096	~89 M20K
Arria 10 (up to Gen 2 10Gbps interface)	~13655 ALM	~599296	~93 M20K
Cyclone 10 (up to Gen 2 10Gbps interface)	~13702 ALM	~599296	~93 M20K
Arria V (up to Gen 1 5Gbps interface)	~5216 ALM	~457536	~81 M10K
Cyclone V (up to Gen 1 5Gbps interface)	~5245 ALM	~457008	~78 M10K

Notes:
(1) Core LE Usage summary is based on 1 - Bulk IN and 1 - Bulk OUT endpoints with 16K buffer each.
(2) For Gen2x2 mode, Cyclone 10 and Arria 10 device, the core LE usage summary is based on Protocol layer and Endpoint FIFO data width is set to 256.
(3) For Gen2 mode, Agilex 7, Stratix 10, Cyclone 10 and Arria 10 device, the core LE usage summary is based on Protocol layer and Endpoint FIFO data width is set to 128.
(4) For Cyclone V and Arria V device, the core LE usage summary is based on Protocol layer and Endpoint FIFO data width is set to 64.
(5) Agilex 7 device support is preliminary.

Deliverables

Contents	Eval	Full
OpenCore Plus Evaluation: One (1) month evaluation license at free of cost	✓	
Full Version: Project based perpetual License with one (1) year post-sales support. Other licensing schemes are also available.		✓
Time-limited (4 hours) SOF generation support	✓	
Full programming files generation support		✓
Encrypted IP Core design files with Control, 1-Bulk IN and 1-Bulk OUT endpoints	✓	✓
Quartus Reference design for Altera® Development Board	✓	✓
Demonstrations: 1) Enumeration Demo 2) Mass Storage Demo 3) UVC Demo 4) Loopback Test Demo	✓	✓
Nios II Sample Applications (with C code) 1) Enumeration	✓	✓
Documentation: 1) IP Core User Guide 2) Windows API User Guide	✓	✓
Windows Reference Driver (Object Code)	✓	✓
Software Library 1) VC++	✓	✓

Support

- IP integration support is available with the purchase of full version.
- IP Core customizing support is available at additional cost.

Contact info@slscorp.com for more information and sales@slscorp.com for placing an order.

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