IP Core

USB 3.2 Gen 2 Device - Software Enumeration, FIFO Interface

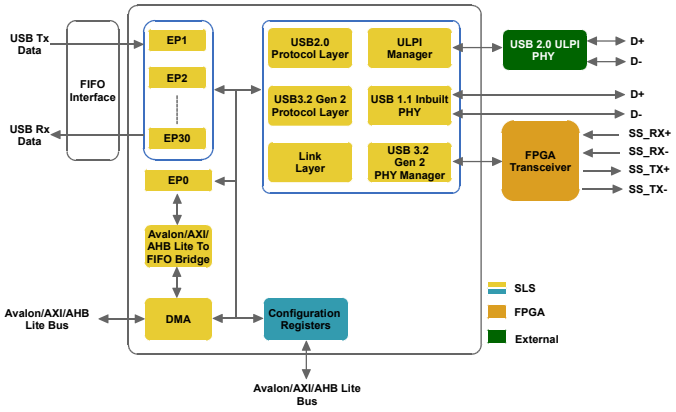
A one-stop solution for USB 3.2 and USB 2.0

Universal Serial Bus or USB has been around for a long time and it is useful to connect a wide variety of devices from storage to input hardware. The purpose of USB is to connect external devices easily by creating a standardized connector to replace the multitude of connectors at the back of a PC.

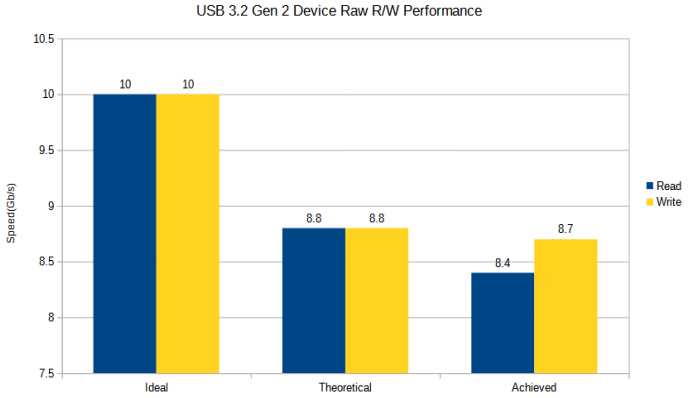
Leveraging the benefits of USB 3.2 Gen 1 device controller, USB 3.2 Gen 2 is designed using the FPGA built-in transceiver. It is a one-stop solution for all USB requirements ranging from USB 3.2 to USB 2.0. It supports SuperSpeed+ (SSP), SuperSpeed (SS), High Speed (HS) and Full Speed (FS) communication modes. The Core architecture allows to use minimal pins from FPGA for USB 3.2 interface with better stability. It provides USB 2.0 backward compatibility using an external USB 2.0 ULPI PHY.

It has been designed to provide simplicity and flexibility along with highest throughput i.e. >8Gbps. Avalon/AXI/AHB Lite interface allows to manage the control transfer using software, provides flexibility, while FIFO interface allows to transfer the data over non-control endpoint ensuring highest throughput.

Architecture



Performance Result



Features

- USB 3.2 Specific Features
  - Supports SuperSpeedPlus (SSP - USB 3.2 Gen 2) and SuperSpeed (SS - USB3.2 Gen 1) mode
  - Uses FPGA Transceiver as a PHY layer and thus eliminates need for external PHY for USB 3.2
- USB 2.0 Specific Features
  - Supports High Speed (HS) and Full Speed (FS) modes
  - Provides well known ULPI interface to interact with external USB 2.0 PHY
  - Supports Low Power Management (LPM)
  - Supports inbuilt PHY for FS and LS modes
- Ease of Use
  - Simple FIFO interface to transfer data over non-control endpoint
- Flexibility
  - Capable to support up to 31 endpoints (1 default control endpoint, 15 IN endpoints and 15 OUT endpoints)
  - Allows to select number of buffers per endpoint based on the requirement

Application

- Imaging Device
- Machine Vision
- Storage Device
- Data Centers

Licensing

- **OpenCore Plus Evaluation**: 1 month evaluation license at no cost
- **Full**: Project based Perpetual License
- **Annual Maintenance**: 20% of License fee from next year to continue technical support and getting updates of IP Core

Deliverable

Contents	Eval	Full
OpenCore Plus Evaluation: One (1) month evaluation license at free of cost	✓	
Full Version: Project based perpetual License with one (1) year post-sales support. Other licensing schemes are also available.		✓
Time-limited (1 hour) JOB file generation support	✓	
Full programming files generation support		✓
Encrypted IP Core design files with Control, 1-Bulk IN and 1-Bulk OUT endpoints	✓	✓
Reference design for FPGA Evaluation Board and SLS FMC eUSB 3.1 Snap On Board	✓	✓
Demonstrations: 1) Streaming Test Demo 2) Loopback Test Demo	✓	✓
Processor Sample Applications (with C code) 1) Enumeration	✓	✓
Documentation: 1) IP Core User Guide 2) Windows API User Guide	✓	✓
Windows Reference Driver (Object Code)	✓	✓
Device Endpoint's FIFO Interface Simulation Model	✓	✓

Support

- IP integration support is available with the purchase of full version
- Additional support on chargeable basis for a period of 3 months or more
- IP Core modification support available at additional cost

Contact info@slscorp.com for more information and sales@slscorp.com for placing an order.

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