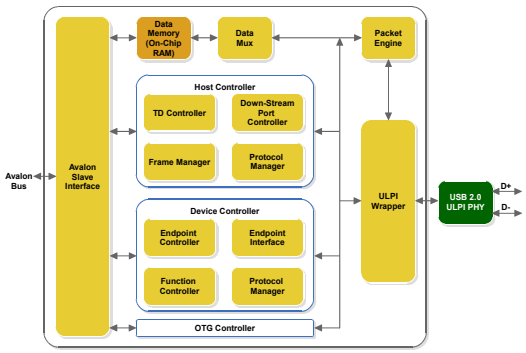
IP Core

USB 2.0 On-The-Go (USB20OTG)

The USB 2.0 On-The-Go (OTG) IP Core is a 32-bit Avalon interface compliant core and supports ULPI interface. It supports both USB Host and USB Device peripheral functionality. While acting as USB Host, it supports High Speed (HS), Full Speed (FS) and Low Speed (LS) modes. While acting as USB Device peripheral, it supports High Speed (HS) and Full Speed (FS) modes.

IP core has been implemented in Verilog HDL and its functionality has been verified using different test cases in simulation environment as well as on hardware. It is provided as Altera Qsys Ready component and hence can be easily integrated in Qsys system.

Architecture



Features

- Supports UTMI + Low Pin interface (ULPI) interface
- Supports Asynchronous Avalon clock interface
- Configurable Memory depth
- Supports software controlled PHY register access
- Configurable to use as HOST only mode or DEVICE only mode
- Ready to use component for Qsys
- Meets Altera Design Assistant guidelines
- Host Controller
  - Supports Low speed (1.5 Mbps), Full speed (12 Mbps) and High Speed (480 Mbps) modes
  - Supports Control, Bulk and Interrupt transfers
  - Supports PING protocol
  - Supports SPLIT transaction for High Speed hub
  - Optimized TD (Transfer Descriptor) structure
  - Supports 16 Interrupt and 16 Aperiodic TDs
- Device (Peripheral) Controller
  - Supports Full speed (12 Mbps) and High Speed (480 Mbps) modes
  - Supports Control, Bulk, Interrupt and Isochronous transfers
  - Capable to support up to 31 endpoints (1 default control end-point + 15 IN/OUT endpoints)
  - Supports software configurable endpoints
  - Supports Suspend, Resume and Remote Wakeup features

Verification

- IP Core has been tested by interfacing it with USB 2.0 PHY (RN1133) on SLS HSIC development board.
- It has also been verified under simulation environment.

Support

- IP integration support available with the purchase of full version
- Additional support on chargeable basis for a period of 3 months or more
- IP Core modification support available at additional cost

Implementation Results

Supported Families	Mode	Resource Utilization	Performance (Fmax) MHz	Memory Bits
Cyclone III	OTG	4775 LE	82.99	131072
	DEVICE	2162 LE	81.81	131072
	HOST	3080 LE	82.24	131072
Cyclone IV GX	OTG	4768 LE	77.15	131072
	DEVICE	2164 LE	77	131072
	HOST	3077 LE	77.15	131072
Cyclone V	OTG	2060 ALM	66.56	131072
	DEVICE	988.5 ALM	66.6	131072
	HOST	3125 ALM	66.3	131072

Note: IP core contains parameter to select mode of operation. This allows resource optimization based on requirement. User can choose any of the following modes: OTG (supports both host and peripheral functionality), DEVICE (supports peripheral functionality only) and HOST (supports host functionality only).

Deliverables

Contents	Eval	Full
OpenCore Plus Evaluation: One (1) month evaluation license at no cost	✓	
Full Version: One (1) Year development license with full version purchase for single project and single site. Other licensing schemes are also available.		✓
Demonstrations: 1) Device Enumeration	✓	✓
Time-limited (4 hours) SOF generation support	✓	
Full programming files generation support		✓
Reference Design for HSIC Development Board	✓	✓
USB 2.0 Host BFM simulation model for Altera Modelsim	✓	✓
Linux (v3.4) based sample application files and Drivers	✓	✓
Windows example files and Drivers (object code)	✓	✓
Documentation: 1) IP Core User Guide 2) Host BFM User Guide	✓	✓

Licensing

- **OpenCore Plus Evaluation**: 1 month evaluation license at no cost
- **Full**: 1 Year development license with full version purchase for single project and single site
- **Renewal**: OpenCore Plus Evaluation license update at discounted price

Download the evaluation version for the core from http://www.slscorp.com/ip-cores/communication/usb-2-0-on-the-go-usb20otg.html

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