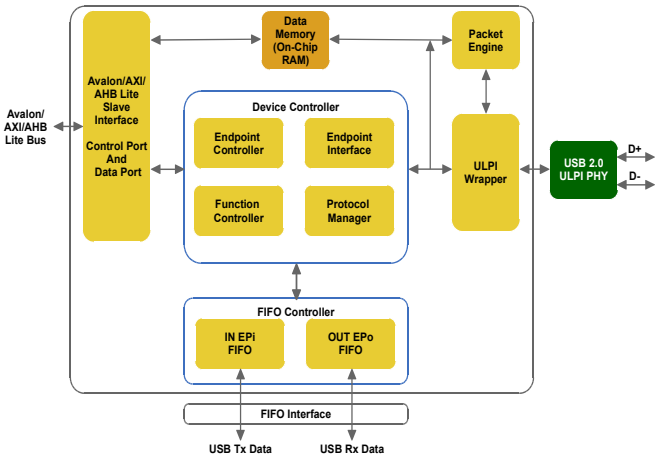
IP Core

USB 2.0 Device - Software Enumeration FIFO Interface (USB20SF)

The USB 2.0 Device, Software Enumeration FIFO interface (USB20SF) IP Core is a FIFO based USB 2.0 device core with 32-bit Avalon/AXI/AHB Lite interface and ULPI interface support. The core supports High Speed (480 Mbps), Full Speed (12 Mbps) and Low Speed (1.5 Mbps) functionality. The core supports three preconfigured endpoints - Control, IN, and OUT. It can be configured for upto 15 IN as well as OUT endpoints on customer's request at additional cost.

IP core has been implemented in Verilog HDL and its functionality has been verified using different test cases in simulation environment as well as on hardware. It is provided as Ready component and hence can be easily integrated in FPGA design system.

Architecture



Features

- Supports High Speed (480 Mbps), Full Speed (12 Mbps) and Low Speed (1.5 Mbps) modes
- Supports Control, Bulk, Interrupt and Isochronous transfers
- Capable to support up to 31 endpoints
  (1 default control endpoint + 15 IN/OUT endpoints)
- Supports software configurable endpoints
- Supports Suspend and Resume features
- Supports UTMI + Low Pin interface (ULPI) interface
- Supports Asynchronous Avalon/AXI/AHB Lite clock interface
- Preconfigured for 3 endpoints
  - CONTROL
  - IN
  - OUT
- Software controlled CONTROL endpoint
- Support LPM (Advanced Suspend Mode) Mode
- Supports Asynchronous FIFO Interface for non CONTROL endpoint
- Supports software controlled PHY register access
- Ready to use component for FPGA design tools
- Optimized for use with embedded processor
- Optimized resource count

Verification

- IP Core has been tested by interfacing it with USB 2.0 PHY on various FPGA development boards.
- USB20SF IP core's functionality is verified in simulation software using test bench written in Verilog HDL.

Deliverables

Contents	Eval	Full
OpenCore Plus Evaluation: One (1) month evaluation license at no cost	✓	
Full Version: Project based perpetual License with one (1) year post sales support. Other licensing schemes are also available.		✓
Demonstrations: 1) Streaming 2) Loop-back	✓	✓
Time-limited (4 hours) SOF generation support	✓	
Full programming files generation support		✓
Reference Design for FPGA Development Board	✓	✓
USB 2.0 Host BFM simulation model	✓	✓
Embedded processor sample applications (with C code): 1) Streaming	✓	✓
HAL Driver object code	✓	✓
Windows Reference Drivers (object code)	✓	✓
Software Library: 1) VC++	✓	✓
Utilities: 1) WinUSB based Application	✓	✓
Documentation: 1) IP Core User Guide 2) Host BFM User Guide 3) HAL API User Guide 4) Hardware and Simulation Tutorial	✓	✓

Licensing

- **OpenCore Plus Evaluation**: 1 month evaluation license at no cost
- **Full**: Project based Perpetual license
- **Maintenance**: 20% of License fee from next year to continue technical support and getting updates for IP Core

Support

- IP integration support available with the purchase of full version
- IP Core customization support available at additional cost

Contact info@slscorp.com for more information and sales @slscorp.com for placing an order.

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