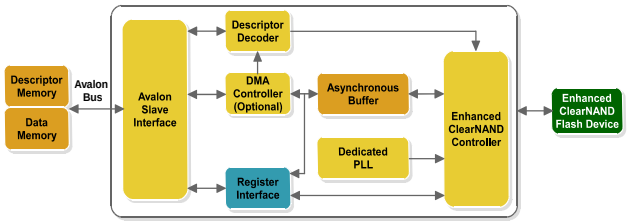
IP Core

Enhanced ClearNAND Controller

Enhanced ClearNAND Controller IP Core is the intermediate stage between NAND Flash memory and master controller. It is designed to have high speed solution to manage NAND Flash application. It supports Open NAND Flash Interface Working Group (ONFI) standard. Two advanced architectures - register based and descriptor based, provides high speed performance, software flexibility, data integrity and device compatibility. Descriptor based architecture reduces amount of CPU intervention.

Enhanced ClearNAND Controller IP Core gives full support for Altera's SOPC Builder and Qsys based systems and provides communication between processor and NAND Flash device using Avalon interface.

Architecture



Fetures

- Supports ONFI EZ NAND 2.3 plus enhanced command set
- Supports integrated 32 bit DMA interface for data transfer
- Supports interrupt driven functionality
- Supports [0-5] asynchronous and [0-5] source synchronous modes of operation
- Supports 8 bit data bus
- Supports command repeat and auto address increment functionality
- Configurable buffer depth
- Multi-Plane (interleave) operation support
- Avalon Bus Compliant

Implementation Results on Cyclone IV E

IP Core Name	Interface	Resource Utilization	Performance (fmax) MHz	Memory Bits
Enhanced ClearNAND Controller (with internal DMA)	Asynchronous	2070 LE	84	4352
	Synchronous	2282 LE	113	4352
Enhanced ClearNAND Controller (without internal DMA)	Asynchronous	1841 LE	84	4096
	Synchronous	2079 LE	116	4096

Licensing

- **OpenCore Plus Evaluation** : 1 month evaluation license at no cost
- **Full** : 1 Year development license with full version purchase for single project and single site
- **Renewal** : OpenCore Plus Evaluation license update at discounted price

Deliverables

Contents	Eval	Full
OpenCore Plus Evaluation: One (1) month evaluation license at no cost	✓	
Full Version: One (1) Year development license with full version purchase for single project and single site. Other licensing schemes also available.		✓
Time-limited (4 hours) SOF generation support	✓	
Full programming files generation support		✓
SLS USB 3.0 Development Board Reference Design	✓	✓
Nios II Sample Applications (with C code): 1) Command Test	✓	✓
Documentation: 1) IP Core User Guide 2) Hardware and Simuation Tutorial	✓	✓

Verification

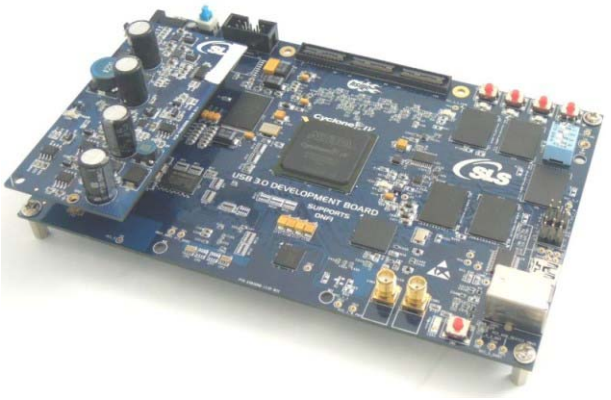
- The IP Core is tested on SLS USB 3.0 Development Board.
- ECNAND Controller IP core's functionality is verified in Altera ModelSim simulation software using test bench written in Verilog HDL.

Support

- IP integration support available with the purchase of full version
- Additional support on chargeable basis for a period of 3 months or more
- Core modification support available at additional cost

USB 3.0 Development Board

SLS has developed USB 3.0 Development Board with ECNAND Flash that can be used to verify the functionality of IP Core.
Contact info@slscorp.com for details.



Note: Enhanced ClearNAND is a registered trade mark of Micron.

Download the evaluation version for the core from http://www.slscorp.com/ip-cores/memory/nand-flash/ecnand-controller.html

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