IP Core

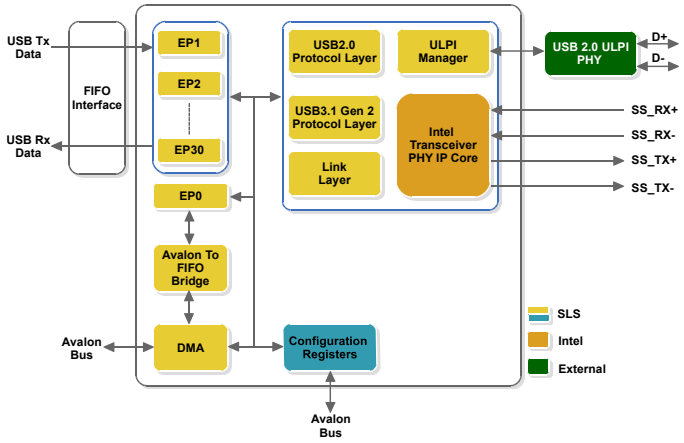
eUSB 3.1 Gen 2 Device - Software Enumeration, FIFO Interface

A one-stop solution for USB 3.1 and USB 2.0

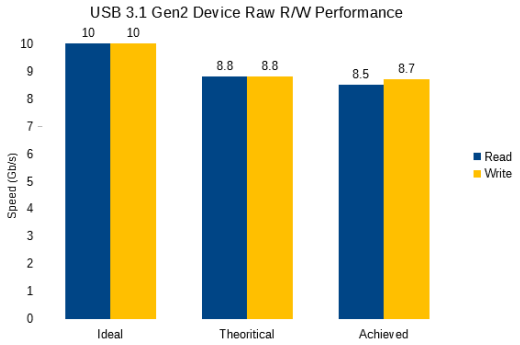
Leveraging the benefits of eUSB 3.0/3.1 Gen 1 device controller, eUSB 3.1 Gen 2 is designed using the Intel® FPGA built-in transceiver. It is a one-stop solution for all USB requirements ranging from USB 3.1 to USB 2.0. It supports SuperSpeed+ (SSP), SuperSpeed (SS), High Speed (HS) and Full Speed (FS) communication modes. The Core architecture allows to use minimal pins from FPGA for USB 3.1 interface with better stability. It provides USB 2.0 backward compatibility using an external USB 2.0 ULPI PHY.

It has been designed to provide simplicity and flexibility along with ***highest throughput i.e. >8Gbps***. Avalon interface allows to manage the control transfer using software, provides flexibility, while FIFO interface allows to transfer the data over non-control endpoint ensuring highest throughput.

Architecture



Performance Results



Check out Video at https://youtu.be/PYzIhbIIN_I

Features

- USB 3.1 Specific Features
  - Supports SuperSpeedPlus (SSP - USB 3.1 Gen 2) and SuperSpeed (SS - USB3.1 Gen 1) mode
  - Uses Intel Transceiver as a PHY layer and thus eliminates need for external PHY for USB 3.1
- USB 2.0 Specific Features
  - Supports High Speed (HS) and Full Speed (FS) modes
  - Provides ULPI interface to interact with external USB 2.0 PHY
- Ease of Use
  - Ready to use component for Intel's Qsys
  - Simple FIFO interface to transfer data over non-control endpoint
- Flexibility
  - Capable to support up to 31 endpoints (1 default control endpoint, 15 IN endpoints and 15 OUT endpoints)
  - Allows to select number of buffers per endpoint based on the requirement

Implementation Results

Device	Resources	Memory Bits	Memory Blocks
Stratix 10 (up to Gen 2 10Gbps Interface)	~19300 ALM	~631200	~92 M20K
Arria 10 (up to Gen 2 10Gbps interface)	~17455 ALM	~729856	~99 M20K
Cyclone 10 (up to Gen 2 10Gbps interface)	~18250 ALM	~729856	~99 M20K
Arria V (up to Gen 1 5Gbps interface)	~4973 ALM	~481424	~86 M10K
Cyclone V (up to Gen 1 5Gbps interface)	~5007 ALM	~480896	~83 M10K
Note: Core LE Usage summary is based on 1 - Bulk IN and 1 - Bulk OUT endpoints with 16K buffer each.			

Deliverable

Contents	Eval	Full
OpenCore Plus Evaluation: One (1) month evaluation license at free of cost	✓	
Full Version: Project based perpetual License with one (1) year post-sales support. Other licensing schemes are also available.		✓
Time-limited (4 hours) SOF generation support	✓	
Full programming files generation support		✓
Encrypted IP Core design files with Control, 1-Bulk IN and 1-Bulk OUT endpoints	✓	✓
Quartus Reference design for Intel® Development Board	✓	✓
Demonstrations: 1) Enumeration Demo 2) Mass Storage Demo 3) UVC Demo 4) Loopback Test Demo	✓	✓
Nios II Sample Applications (with C code) 1) Enumeration	✓	✓
Documentation: 1) IP Core User Guide 2) Windows API User Guide	✓	✓
Windows Reference Driver (Object Code)	✓	✓
Software Library 1) VC++	✓	✓

Application

- Imaging Device
- Storage Device
- Machine Vision
- Data Centers

Licensing

- **OpenCore Plus Evaluation**: 1 month evaluation license at no cost
- **Full**: Project based Perpetual License
- **Maintenance**: 20% of License fee from next year to continue technical support and getting updates for IP Core

Support

- IP integration support is available with the purchase of full version
- IP Core customization support available at additional cost

Contact info@slscorp.com for more information and sales@slscorp.com for placing an order.

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