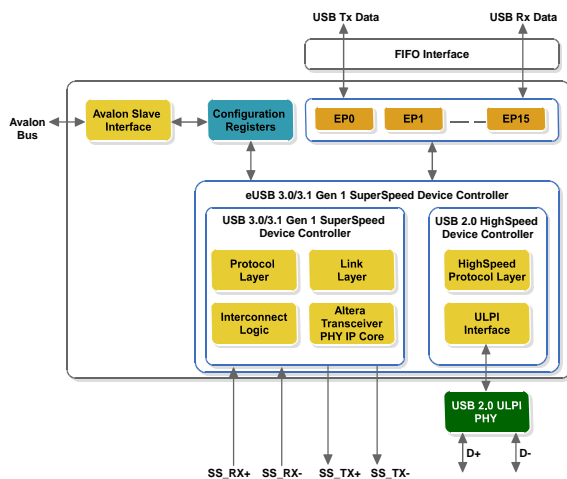# IP Core
eUSB 3.0/3.1 Gen 1 Device

The integration of USB 3.0 3.1 Gen 1 Device with FPGA development board needs 60+ I/O for USB 3.0/3.1 Gen 1 PHY chip to connect it with FPGA. This adds an extra cost to the board. Altera has introduce the FPGA which has in built transceiver which run at 5Gbps speed (same as USB 3.0/3.1 Gen 1 Specification) with features like 8b/10b, SKIP control etc. required during implementing USB 3.0/3.1 Gen 1 Controller. SLS has integrate the USB 3.0/3.1 Gen 1 Device IP Core with the Altera Transceiver and USB 2.0 PHY chip, and developed the eUSB 3.0/3.1 Gen 1 Device Controller IP Core, offering low cost solution.

The eUSB 3.0/3.1 Gen 1 Device Controller IP Core is SuperSpeed Core developed by SLS to provide better solutions and options to user for implementation of USB 3.0/3.1 Gen 1 interface in their design. There is no need for external USB 3.0/3.1 Gen 1 PHY chip because IP Core supports SuperSpeed operation with Altera Transceiver running at 5Gbps in FPGA and High Speed operation with external USB 2.0 Transceiver PHY chip. This will reduces the I/O pin for USB 3.0/3.1 Gen 1 connection from 60+ to 18 and also saves board space. This provides a compatible link to both USB 3.0/3.1 Gen 1 and USB 2.0 Device for an embedded applications. The SLS eUSB 3.0 HSMC Snap On Board provides a platform for verification and testing of the IP Core.

Architecture

Implementation Results

Supported Family	Resource Utilization	Memory Bits	Memory Blocks
Cyclone V GT/ST SoC	6000 ALM	300000	39 M10K
Stratix V GX/GS/GT	6200 ALM	300000	26 M20K
Arria V GX/GT/GZ/SX SoC/ST SoC	5800 ALM	300000	42 M10K

Deliverables

Contents	Eval	Full
eUSB3.0 Development Board		✓
OpenCore Plus Evaluation: One (1) month evaluation license at no cost	✓	
Full Version: One (1) Year development license with full version purchase for single project and single site. Other licensing schemes also available.		✓
Time-limited (4 hours) SOF generation support	✓	
Full programming files generation support		✓
Qsys based Reference designs for Altera Cyclone V GT Development Board	✓	✓
Demonstrations: 1) Enumeration Demo 2) Mass Storage Demo	✓	✓
Nios II Sample Applications (with C code) 1) Enumeration	✓	✓
Documentation: 1) IP Core User Guide	✓	✓
Windows Reference Driver (Object Code)	✓	✓
Software Library 1) VC++	✓	✓
Utilities 1) USB View	✓	✓

Features

- Supports SuperSpeed operation with Altera Transceiver running at 5Gbps in FPGA and High Speed operation with External USB 2.0 Transceiver PHY chip
- Implementation of PHY Layer (with Altera 5Gbps Transceiver), Link Layer and Protocol Layer
- Supports 8b/10b, SKIP Control
- Supports configurable Endpoint selection
- Avalon bus compliant
- Complete software based control for device enumeration and control request

eUSB3.0 Development Board

- Altera Cyclone V GT FPGA
- Six B-Type USB 3.0 Connector
- DDR2, SDRAM, CFI Flash, 64 Mbit Serial Configuration (EPCS64) EEPROM
- HSMC Connector
- Four Push Button Switche
- Three user-defined LEDs
- SD Card Socket

eUSB 3.0 HSMC Snap On Board

- Standard HSMC Interface
- Two USB 3.0/3.1 Gen 1 Micro AB-type connectors
- Two USB 3.0/3.1 Gen 1 B-type connectors
- Six user-defined IOs
- Three user-defined LEDs

Application

- USB 3.0/3.1 Gen 1 Device based applications
- USB 2.0 Device/Host/OTG based applications

Licensing

- OpenCore Plus Evaluation: 1 month evaluation license at no cost
- **Full**: 1 Year development license with full version purchase for single project and single site
- **Renewal**: OpenCore Plus Evaluation license update at discounted price

Support

- IP integration support available with the purchase of full version
- Additional support on chargeable basis for a period of 3 months or more
- IP Core modification support available at additional cost

Contact info@slscorp.com for more information and sales @slscorp.com for placing an order.