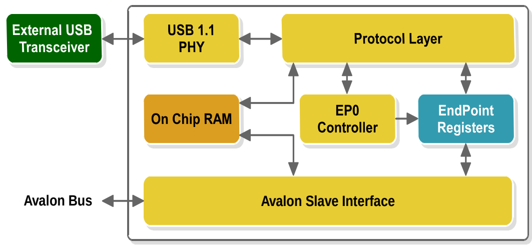
IP Core

USB 1.1 Device, Software Based Enumeration (USB11SR)

The USB 1.1 Device, Software Based Enumeration IP Core is RAM based USB 1.1 device core with 32-bits Avalon interface. The core supports Full Speed (12 Mbps) functionality and Low Speed (1.5 Mbps) functionality can be added as per customer request with additional charges. The core supports three preconfigured Control, Bulk IN and Bulk OUT endpoints. It can be configurable for up to 15 IN/OUT endpoints on customer request on chargeable basis. Each configurable endpoints has an endpoint controller that supports Interrupt, Bulk and Isochronous transfers.

The core has been optimized for Altera FPGAs and its functionality has been verified on the hardware with Altera Quartus II. The package includes ModelSim precompiled library for core simulation and verification.

Architecture



Features

- Verilog Implementation on RTL level
- Supports Full-speed (12 Mbps) transfer rate
- Software based USB enumeration Support
- Avalon Interconnection compliant
- Preconfigured for 3 endpoints
  - CONTROL
  - BULK IN
  - BULK OUT
- Configurable for up to 15 IN/OUT endpoints which supports Bulk, Isochronous and Interrupt functionality on customer request at additional cost
- Cyclic redundancy code (CRC) checking/generation
- Data toggle synchronization mechanism
- Optimized for use with Altera Nios II embedded processor

Implementation Results

Supported Families	Resource Utilization	Performance (Fmax) MHz	Memory Blocks
Cyclone III	1900 LE	103	8 M9K
Cyclone IV	1900 LE	109	8 M9K
Cyclone V	840 ALM	60	8 M10K
Stratix III	1300 ALUT	141	8 M9K
Stratix IV	1300ALUT	130	8 M9K
Stratix V	800 ALM	100	8 M20K
Arria II	1300 ALUT	115	8 M9K
Arria V	830 ALM	83	8 M10K
MAX 10	1900 LE	104	8 M9K
Note: The implementation results may change upon core revision			

Licensing

- **OpenCore Plus Evaluation**: 1 month evaluation license at no cost
- **Full**: 1 Year development license with full version purchase for single project and single site
- **Renewal**: OpenCore Plus Evaluation license update at discounted price

Deliverables

Contents	Eval	Full
OpenCore Plus Evaluation: One (1) month evaluation license at no cost	✓	
Full Version: One (1) Year development license with full version purchase for single project and single site. Other licensing schemes are also available.		✓
Time-limited (4 hours) SOF generation support	✓	
Full programming files generation support for ESDK 1C12 Board		✓
Simulation library for Enumeration process	✓	✓
Demonstration: (1) Mass Storage (2) Port Interface (3) Performance Test (Streaming Bulk IN and Bulk OUT) (4) CDC Serial	✓	✓
Drivers: (1) HAL Driver (Compiled version) (2) Windows Driver (Compiled version)	✓	✓
Software Library: 1) VC++	✓	✓
Nios II Application (1) Port Interface (2) Streaming	✓	✓
Utilities: 1) USBView 2) Port Interface	✓	✓
Documentation: 1) IP Core User Guide 2) HAL API User Guide 3) Hardware Tutorial	✓	✓

Verification

- USB11SR Device core's functionality is verified in ModelSim simulation software using test bench written in Verilog HDL.
- USB11SR IP is also tested by interfacing with USB 1.1 PHY chip on SLS ESDK 1C12 Board.

Support

- IP integration support available with the purchase of full version
- Additional support on chargeable basis for a period of 3 months or more
- IP Core modification support available at additional cost

Download the evaluation version for the core from http://www.slscorp.com/ip-cores/communication/usb-11-device/usb11srsoft.html

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