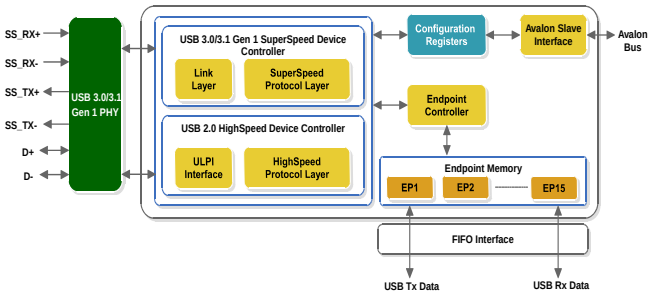
IP Core
USB 3.0/3.1 Gen 1 Device

The SLS USB 3.0/3.1 Gen 1 Device core is the SuperSpeed core that supports connectivity between TI USB 3.0/3.1 Gen 1 PHY (TUSB1310A) and Altera FPGA. The Core is wrapped around with software drivers and examples for its ease of use and quick integration. The ready to use Development board availability makes the integration faster. The core package also contains the reference design that can be used directly for starting a custom application development.

The core has been optimized for Altera FPGAs and its functionality has been verified on the hardware with Altera Quartus II. The package includes ModelSim precompiled library for core simulation and verification.

Architecture



Features

- Implementation of Link Layer and Protocol Layer
- Support 16-bit and 32-bit PHY layer data interface
- Supports CONTROL, BULK and ISO transfer without stream support
- USB 2.0 backward compatible
- All Link layer power state handling
- Implements CRC calculation and generation in hardware
- Configurable Endpoint selection

Development Board

- Cyclone IV E FPGA
- Texas USB1310A PHY
- USB UART Connector
- 1 Gb DDR2 SDRAM
- 64 Mbit SDR SDRAM
- 64 Mbit CFI Flash
- HSMC Connector
- µSD Card Reader
- Micro SD Card Connector
- GPIO Headers
- 4-way DIP Switch
- Four Push Button Switches
- Four user-defined LEDs
- Five NAND FLASH
- Device (optional)

Verification

- USB 3.0/3.1 Gen 1 Device IP core's functionality is verified in ModelSim simulation software using test bench written in Verilog HDL

Support

- IP integration support available with the purchase of full version
- Additional support on chargeable basis for 3 months or more Core modification support available at additional cost

Implementation Results

Supported Families	Resource Utilization	Performance (fmax) MHz	Memory Blocks
Cyclone IV	10000 LE	250	36 M9K
Cyclone V	4710 ALM	405	35 M10K
Stratix IV	5215 ALUT	412	33 M9k
Stratix V	4797 ALM	717.36	10 M20K
Arria V	4703 ALM	338.41	35 M10K
MAX 10	10000 LE	250	36 M9K

Deliverables

Contents	Eval	Full
OpenCore Plus Evaluation: One (1) month evaluation license at no cost	✓	
Full Version: One (1) Year development license with full version purchase for single project and single site. Other licensing schemes also available.		✓
Time-limited (4 hours) SOF generation support	✓	
Full programming files generation support		✓
Reference designs for SLS USB 3.0 Development Board 1) SOPC based 2) Qsys based	✓	✓
Demonstrations: 1) USB Enumeration 2) USB Mass Storage Device Class 3) YUV2 Camera	✓	✓
Simulation library for Altera ModelSim version	✓	✓
Nios II Sample Applications (with C code) 1) Enumeration	✓	✓
Documentation: 1) IP Core User Guide 2) Windows API User Guide	✓	✓
Windows Reference Driver (Object Code)	✓	✓
Software Library 1) VC++	✓	✓
Utilities 1) USB View 2) Amcap	✓	✓

Licensing

- OpenCore Plus Evaluation: 1 month evaluation license at no cost
- **Full**: 1 Year development license with full version purchase for single project and single site
- **Renewal**: OpenCore Plus Evaluation license update at discounted price

Download the evaluation version for the core from http://www.slscorp.com/ip-cores/communication/usb-30-device.html

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