

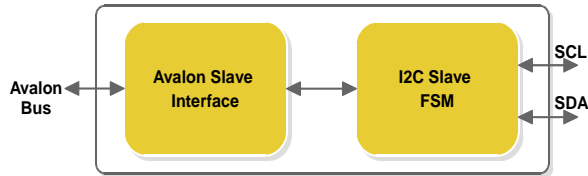
IP Core

I²C Slave

The I²C slave IP is fully synthesizable core and compatible with Phillips I²C standard. The IP uses I²C Bus Protocol which helps maximize the hardware efficiency and minimize the interfaces.

It is provided as Altera SOPC Builder ready component and integrates easily into any SOPC Builder generated system.

Architecture



Features

- Data transfer up to 100 Kbps in standard mode and up to 400 Kbps in fast-mode
- Uses two wires to transfer information between devices
- Bi-directional data transfer
- 7-bit addressing format
- Fixed data width of 8 bits
- Data transfer in multiples of bytes
- Interrupt or bit-polling driven byte-by-byte data transfer
- Start/Stop detection
- Operates from a wide range of input clock frequency
- Fully synthesizable

Implementation Results

| Supported Families | Resource Utilization | Performance (Fmax) MHz | Memory Bits |
|--------------------|----------------------|------------------------|-------------|
| Cyclone III | 154 LE | 250 | - |
| Cyclone IV | 154 LE | 230 | - |
| Cyclone V | 64 ALM | 275 | - |
| Stratix III | 69 ALUT | 230 | - |
| Stratix IV | 67 ALUT | 400 | - |
| Stratix V | 62 ALM | 390 | - |
| Arria II | 70 ALUT | 260 | - |
| Arria V | 64 ALM | 300 | - |
| MAX 10 | 155 LE | 220 | - |

Note: The implementation results may change upon core revision

Deliverables

| Contents | Eval | Full |
|---|------|------|
| OpenCore Plus Evaluation: One (1) month evaluation license at no cost | ✓ | |
| Full Version: One (1) Year development license with full version purchase for single project and single site. Note: Other licensing schemes are also available. | | ✓ |
| Time-limited (4 hours) SOF generation support for UP3 1C6 board | ✓ | |
| Full programming files generation support for UP3 1C6 board | | ✓ |
| I2C Slave application | ✓ | ✓ |
| Documentation: 1) IP Core user guide 2) Hardware and Simulation tutorial 3) HAL API user guide | ✓ | ✓ |

Applications

- Serial communication applications

Verification

- I2C Slave IP Core's functionality is verified in Modelsim simulation software using test bench in Verilog HDL.

Support

- IP integration support available with the purchase of full version
- Additional support on chargeable basis for a period of 3 months or more
- Core modification support available at additional cost

Licensing

- **OpenCore Plus Evaluation** : 1 month evaluation license at no cost
- **Full** : 1 Year development license with full version purchase for single project and single site
- **Renewal** : OpenCore Plus Evaluation license update at discounted price

Download the evaluation version for the core from <http://www.slscorp.com/ip-cores/interface/i2c-slave.html>