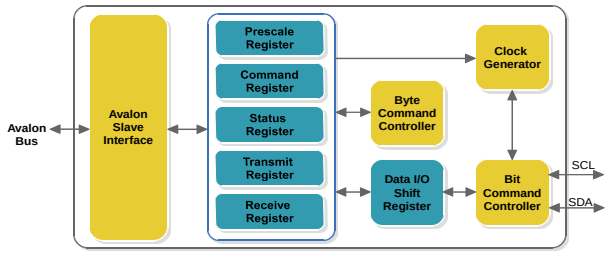
IP Core

I²C Master

Avalon compliant I²C Master IP core provides an interface between Nios II processor and an I²C Slave device. It can work as a master transmitter or master receiver depending on working mode determined by Nios II processor. The core incorporates all features required by the latest I²C specification including clock synchronization, arbitration, multi-master systems and Fast-speed transmission mode.

It is provided as Altera SOPC Builder ready component and integrates easily into any SOPC Builder generated system.

Architecture



Features

- Compatible with Philips I²C standard
- Two transmission speeds are supported; Normal: 100Kbps Fast: 400Kbps
- Multi Master Operation
- Software programmable clock frequency
- Clock Stretching and Wait state generation
- Software programmable acknowledge bit
- Interrupt or bit-polling driven byte-by-byte data-transfers
- Arbitration lost interrupt, with automatic transfer cancellation
- Start/Stop/Repeated Start/Acknowledge generation
- Start/Stop/Repeated Start detection
- Bus busy detection
- Supports 7 and 10bit addressing mode
- Operates from a wide range of input clock frequencies
- Static synchronous design

Implementation Results

Supported Family	Resource Utilization	Performance (Fmax) MHz	Memory Bits
Cyclone III	228 LE	170	-
Cyclone IV	227 LE	120	-
Cyclone V	108 ALM	235	-
Stratix III	115 ALUT	200	-
Stratix IV	112 ALUT	275	-
Stratix V	106 ALM	325	-
Arria II	120 ALUT	150	-
Arria V	108 ALM	320	-
MAX 10	227 LE	170	-
Note: The implementation results may change upon core revision			

Deliverables

Contents	Eval	Full
OpenCore Plus Evaluation: One (1) month evaluation license at no cost	✓	
Full Version: One (1) Year development license with full version purchase for single project and single site. Note: Other licensing schemes are also available.		✓
Time-limited (4 hours) SOF generation support for ESDK 1C6 kit	✓	
Full programming files generation support for ESDK 1C6 kit		✓
Nios II Application 1. RTC application without Interrupt 2. RTC application with Interrupt	✓	✓
Simulation library for Altera-Modelsim v6.3g_p1	✓	✓
HAL driver (Source Code)	✓	✓
Documentation: 1) IP Core user guide 2) Hardware and Simulation tutorial 3) HAL API user guide	✓	✓

Applications

- Interface with microcontroller
- Communication System

Verification

- I²C Master Core's functionality is verified in modelsim simulation software using test bench written in Verilog HDL.
- I²C Master IP is also tested by interfacing with RTC (Real Time Clock) and I²C EPROM on SLS UP3 Board.

Support

- IP integration support available with the purchase of full version
- Additional support on chargeable basis for a period of 3 months or more
- Core modification support available at additional cost

Licensing

- **OpenCore Plus Evaluation** : 1 month evaluation license at no cost
- **Full** : 1 Year development license with full version purchase for single project and single site
- **Renewal** : OpenCore Plus Evaluation license update at discounted price

Download the evaluation version for the core from http://www.slscorp.com/ip-cores/interface/i2c-master.html

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