# IP Core

I^{2}C Controller

I^{2}C (Inter-Integrated Circuit) Controller is a two-wire, bi-directional serial bus that provides simple and efficient method of data transmission over a short distance between many devices. Avalon compliant I^{2}C Controller provides an interface between Nios II processor and I^{2}C device. It can work as Master/Slave transmitter or Master/Slave receiver depending on working mode determined by Nios II processor. The I^{2}C Controller IP core incorporates all features required by the latest I^{2}C specification including clock synchronization, arbitration, multi-master systems and Fast-speed transmission mode.

It is provided as Altera SOPC Builder ready component and integrates easily into any SOPC Builder generated system.

Architecture
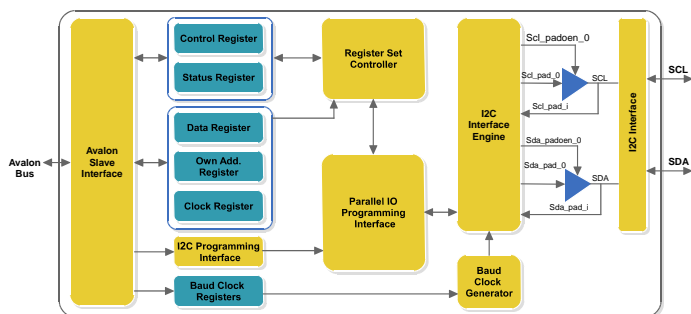
Fetures

- Compatible with Philips I^{2}C(PCF 8584) standard
- Supports both Master and Slave mode
- Automatic detection and adoption to bus interface type
- Multi-master operation
- Byte-by-byte data-transfer is driven by Interrupt or Bit-polling
- Arbitration-lost interrupt with automatic transfer cancellation
- Start/Stop/Repeated Start/Acknowledge generation
- Start/Stop/Repeated Start detection
- Bus-Busy detection
- Supports 7 bit addressing mode
- Operates from wide range of input clock frequencies
- Static synchronous design
- Avalon bus compliant

Implementation Results

Supported Families	Resource Utilization	Performance (Fmax) MHz	Memory Bits
Cyclone III	300 LE	170	-
Cyclone IV	300 LE	170	-
Cyclone V	300 LE	170	-
Stratix III	210 LE	200	-
Stratix IV	210 LE	200	-
Stratix V	210 LE	200	-
Arria II	155 LE	235	-
Arria V	155 LE	235	-
MAX 10	155 LE	235	-
Note: The implementation results may change upon core revision			

Deliverables

Contents	Eval	Full
OpenCore Plus Evaluation: One (1) month evaluation license at no cost	✓	
Full Version: One (1) Year development license with full version purchase for single project and single site. Note: Other licensing schemes are also available.		✓
Time-limited (4 hours) SOF generation support for ESDK Education Kit	✓	
Full programming files generation support for ESDK Education Kit		✓
Nios II Application 1. I2C Controller application using Interrupt 2. RTC application using interrupt	✓	✓
Simulation library for Altera-Modelsim v6.3g_p1	✓	✓
HAL Driver (Object code)	✓	
HAL Driver (Source code)		✓
Documentation: 1) IP Core user guide 2) Hardware and Simulation tutorial 3) HAL API user guide	✓	✓

Verification

- The SLS I^{2}C Controller IP Core's functionality is verified in ModelSim simulation software using test bench written in verilog HDL.
- The I^{2}C Controller's functionality (as a Master) is tested by interfacing with RTC (Real Time Clock) and I^{2}C EPROM on SLS ESDK Education Kit.
- The I^{2}C Controller's functionality (as a Slave) is tested by communicating with another instance of the same core working as master and also with the SLS I2C Master IP Core on the ESDK Education Kit.

Support

- IP integration support available with the purchase of full version
- Additional support on chargeable basis for a period of 3 months or more
- Core modification support available at additional cost

Licensing

- **OpenCore Plus Evaluation** : 1 month evaluation license at no cost
- **Full** : 1 Year development license with full version purchase for single project and single site
- **Renewal** : OpenCore Plus Evaluation license update at discounted price

Download the evaluation version for the core from http://www.slscorp.com/ip-cores/interface/i2c-controller.html