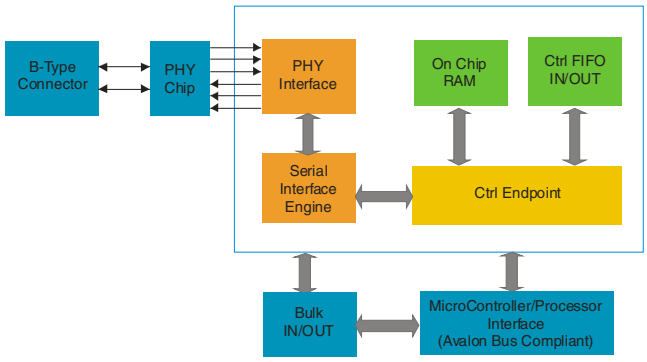
IP Core
USB 1.1

System Level Solutions
Designing Through Innovation

The USB1.1 Device IP core is a universal serial bus (USB) function controller that provides a USB full-speed function interface and meets USB1.1 specification. This IP core is available with 3 standard endpoints (CTRL, BULK IN, and Bulk OUT) configuration with maximum payload size. Each endpoint requires a FIFO to be associated with it. The FIFO size for the Endpoint 0 is fixed at 64 bytes and for Bulk IN and OUT is fixed at 128bytes (64x2 bytes).

It is provided as Altera SOPC Builder ready component and integrates easily into any SOPC Builder generated system.

Architecture



Features

- Verilog Implementation on RTL level
- Supports full-speed (12 Mbps) transfer
- USB enumeration support in harware
- All interfaces are architected using a FIFO based model
- Physical Layer Interface (UTMI compliant)
- Avalon Interconnection compliant
- Extraction clock and data signals in internal digital phase-locked loop (DPLL)
- Cyclic redundancy code (CRC) checking/generation
- Data toggle synchronization mechanism
- Optimized for use with Altera Nios embedded processor

Implementation Results

Supported Family	LEs/ LUTs	Memory Bits	Performance (Fmax) MHz
Cyclone	1195	5120	98
Cyclone II	1188	5120	95
Cyclone III	1201	5120	124
Stratix	1195	5120	90

Note: The implementation results may change upon core revision

Support

- IP integration support available with the purchase of full version
- Additional support on chargeable basis for 3 months or more
- Core modification support available at additional cost

Deliverables

Contents	Eval	Full
OpenCore Plus Evaluation: One (1) month evaluation license at no cost	✓	
Full: One (1) year development license with full version purchase for single project and single site. Note: Other licensing schemes also available.		✓
Time-limited (4 hours) SOF generation support for ESDK 1C12 Education Kit	✓	
Full programming files generation support for ESDK 1C12 Education Kit		✓
Simulation library for Enumeration process	✓	✓
Drivers HAL Driver (Source code) Windows Driver (Compiled version)	✓	✓
Software Library (Compiled version) (1) VC++ (2) C# .net	✓	✓
Nios II Application Port Interface	✓	✓
Utilities Port Interface USB View Enumeration Data Editor	✓	✓
Documentation IP Core user guide Hardware tutorial HAL Driver API Windows Driver API	✓	✓

Verification

- USB1.1 Device core's functionality is verified in ModelSim simulation software using test bench written in Verilog HDL
- USB1.1 IP is also tested by interfacing with USB1.1 PHY chip on SLS ESDK Board

Licensing

- OpenCore Plus : 1 month evaluation license at no cost
- OpenCore : 1 Year development license with full version purchase for single project and single site
- Renewal : OpenCore license update at discounted price

Applications

- Embedded microcontroller systems
- Communication systems

Request Eval Download the evaluation version for the core from http://www.slscorp.com/pages/ipusb1sls.php

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