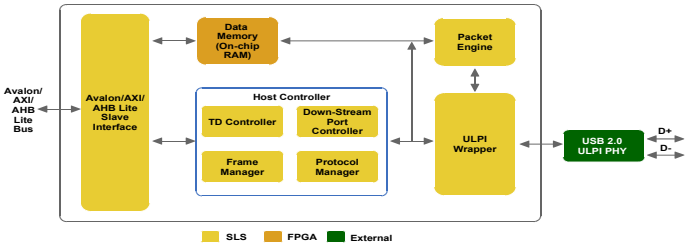
IP Core

USB 2.0 Host Controller (USB20HC)

The USB 2.0 Host Controller IP Core is a 32-bit Avalon/AXI/AHB Lite interface compliant core and supports ULPI interface. It supports High Speed (HS), Full Speed (FS) and Low Speed (LS) modes.

IP core has been implemented in Verilog HDL and its functionality has been verified using different test cases in simulation environment as well as on hardware. It is provided as FPGA ready component and hence can be easily integrated in FPGA design system.

Architecture



Features

- Supports Low Speed (1.5 Mbps), Full Speed (12 Mbps) and High Speed (480 Mbps) modes
- Supports Control, Bulk, Isochronous and Interrupt transfers
- Contains two different interface for Control Port and Data Port to improve Clock Domain Crossing (CDC) performance
- Supports Asynchronous Avalon/AXI/AHB Lite clock interface
  - Enables you to run Avalon/AXI/AHB Lite interface (in turn CPU) at clock frequency independent of ULPI bus
- Supports SPLIT transfer
- Optimized TD (Transfer Descriptor) structure
- Supports PREAMBLE Mode (This mode is used when Low Speed device is connected behind Full Speed hub)
- Supports High Speed high bandwidth Interrupt and Isochronous transfers
- Supports port test modes
- Configurable memory depth
  - Enables you to reduce resource utilization depending on application needs
- Supports UTMI + Low Pin interface (ULPI) interface
- Supports software controlled PHY register access for debugging purpose
- Mass storage class speed performance
  - Upto 14 MBPS speed for read operation
  - Upto 11 MBPS speed for write operation

Verification

- IP Core has been tested by interfacing it with USB 2.0 PHY on various FPGA development boards.
- It has also been verified under simulation environment.

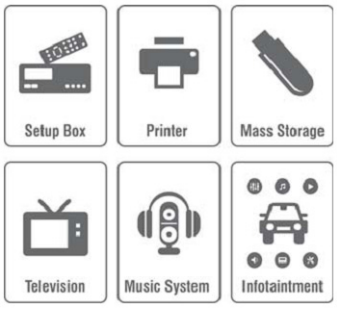
Support

- IP integration support available with the purchase of full version
- IP Core customization support available at additional cost

Deliverables

Contents	Eval	Full
OpenCore Plus Evaluation: One (1) month evaluation license at no cost	✓	
Full Version: Project based perpetual License with one (1) year post sales support. Other licensing schemes are also available.		✓
Demonstrations: 1) Mass Storage 2) Device Enumeration	✓	✓
Time-limited (4 hours) SOF generation support	✓	
Full programming files generation support		✓
Reference Design for FPGA based Development Board	✓	✓
Simulation library	✓	✓
Embedded Processor Sample Applications (with C code): 1) Mass Storage 2) Device Enumeration	✓	✓
HAL Driver object code	✓	✓
Documentation: 1) IP Core User Guide 2) HAL API User Guide 3) Hardware and Simulation User Guide	✓	✓

Applications



Licensing

- **OpenCore Plus Evaluation**: 1 month evaluation license at no cost
- **Full**: Project based Perpetual License
- **Maintenance**: 20% of License fee from next year to continue technical support and getting updates for IP Core

Contact info@slscorp.com for more information and sales@slscorp.com for placing an order.

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