

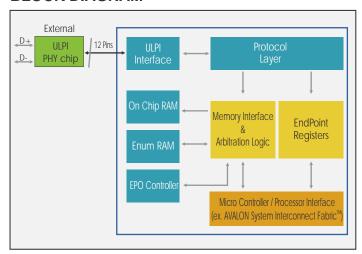


USB 2.0 Device with Avalon Interface - ULPI Support Designing Through Innovation

The USB 2.0 Device with Avalon Interface - ULPI support (USB20HR) IP Core is a RAM based USB IF high-speed certified device core with 32-bit Avalon interface and ULPI interface support. The core supports both High Speed (480 Mbps) and Full Speed (12 Mbps) functionality. The core supports three preconfigured endpoints Control, Bulk IN, and Bulk OUT. It can be configurable for up to 15 IN/OUT endpoints on customer request on chargeable basis. Each configurable endpoint has an endpoint controller that supports interrupt, bulk, and isochronous transfers.

The core has been optimized for Altera FPGAs and its functionality has been verified on the hardware with Altera Quartus II. The package includes ModelSim precompiled library for core simulation and verification.

BLOCK DIAGRAM



FEATURES

- USB 2.0 USB IF high-speed certified (TID# 70680006)
- Supports both High Speed (480 Mbps) and Full Speed (12 Mbps)
- Supported Interfaces
 - ULPI (NXP ISP1504 PHY)
- Preconfigured for 3 endpoints
 - Control Bulk IN Bulk OUT
- Configurable for up to 15 IN/OUT endpoints including Isochronous and Interrupt on customer request at additional cost
- Software controlled USB enumeration
- Optimized for use with Altera[®] Nios[®] II embedded processor
- Avalon System Interconnect Fabric[™] compliant
- Optimized LE count

VERIFICATION

 USB20HR IP core's functionality is verified in ModelSim simulation software using test bench written in Verilog HDL

IMPLEMENTATION RESULTS

IP Core	Supported Families	Interface	LEs	Performance (fmax)	Memory Bits
USB20HR	Cyclone II	ULPI	2520	130 MHz	18432
	Cyclone III	ULPI	2520	135 MHz	18432
	Stratix II	ULPI	2130	173 MHz	18432

Please Note: The implementations results can change upon core revision.

DELIVERABLES

Contents	Eval	Full
CoreCommander Board		1
OpenCore Plus Evaluation: One (1) month evaluation license at no cost	√	
Full Version: One (1) Year development license with full version purchase for single project and single site. Other licensing schemes also available.		1
Demonstrations: 1) Mass Storage 2) Port Interface 3) Performance Test (Streaming Bulk IN and Bulk OUT)	√	√
Time-limited (4 hours) SOF generation support for CoreCommander (3C25) reference design	√	
Full programming files generation support for CoreCommander (3C25) reference design		✓
Simulation library for Modelsim version 6.3g	1	√
Nios II Sample Applications (with C code): 1) Port Interface 2) Streaming	√	1
HAL Driver object code	√	
HAL Driver source code		1
Windows and Linux Reference Drivers (object code)	1	√
Software Library: 1) C#.net 2) VC	√	√
Documentation: 1) IP Core user guide 2) HAL API user guide 3) Windows API user guide 4) Hardware and Simuation Tutorial	√	√
Utilities: 1) Enumeration data editor 2) Port Interface 3) USBView	√	√

SUPPORT

- IP integration support available with the purchase of full version
- Additional support on chargeable basis for 3 months or more
- Core modification support available at additional cost

LICENSING

Download the evaluation version for the core from http://www.slscorp.com/pages/ipusb20hrsls.php

- OpenCore Plus Evaluation: 1 month evaluation license at no cost
- Full: 1 Year development license with full version purchase for single project and single site
- Renewal : OpenCore Plus Evaluation license update at discounted price

Contact info@slscorp.com for more information and sales@slscorp.com for placing an order.

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