Errata Sheet
ONFI2.0 HSMC Board

Board Version: r1b
Document Version: 1.0
Date: June 2014

This document lists the issues related to the ONFI2.0 HSMC Board (rev1b) and its work around.

Issue

Wrong data received when Asynchronous interface device mode 4 (EDO) is configured for the NAND Flash device.

While configuring NAND Flash device in Asynchronous interface device mode 4, it is observed that the data is get delayed due to Level shifter used in data and control signals. This violates the ONFI specification of Asynchronous interface device mode 4 timing. Hence, the wrong data is received at FPGA.

Workaround

By removing the level shifter used for the Read Enable (RE_n) signal delay can be minimized and data can be received correctly. Please make following changes on the board.

1. Remove U5 from the board and short pin 2 with 7 and pin 3 with 8.
2. Change value of R12 resistor from 51K to 475K and R14 resistor from 10K to 140K. This will generate 1.8V instead of 2.5V and it will be used as VCCA of each level shifter.
3. Provide all the NAND Flash interface signals from FPGA side at 1.8V instead of 2.5V.

This issue will be fixed in a future version of the ONFI2.0 HSMC Board. For more information, please contact support@slscorp.com.