Multiple USB Solutions on a Single Chip using MAX10FPGA
Application Note

March 2015, Ver. 1.1

System Level Solutions, Inc. (SLS) is a leading provider of innovative design IPs, VLSI and embedded systems solutions. We here at SLS strive to research on the upcoming technology and solution which provide ease of use to consumers with a better migration to conventional resources. In the same context, we had research on the configurable single chip FPGA device which comes into existence due to its versatile nature. The abstract of research is presented below.

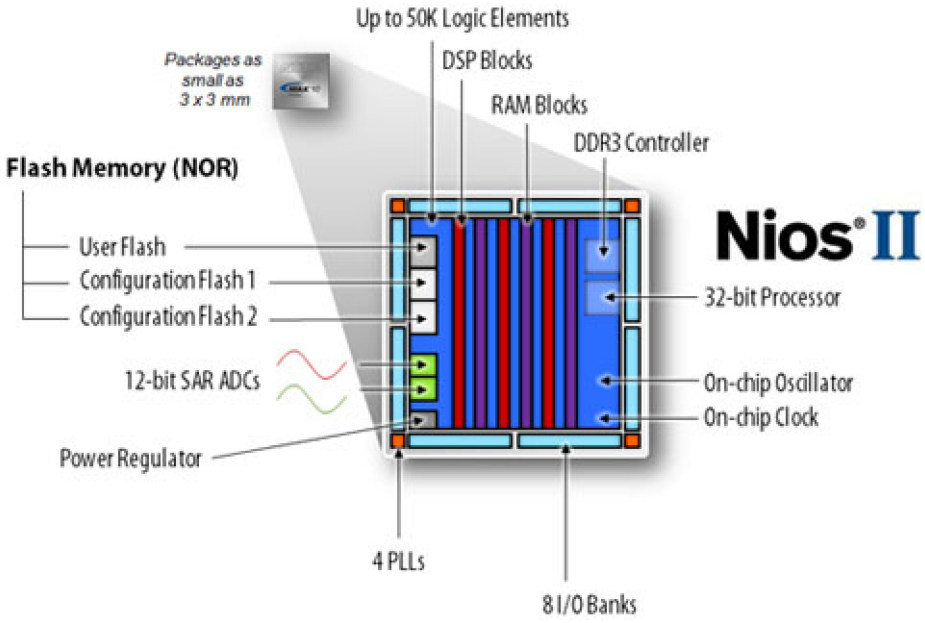
Single chip low scale technology emerged from the increasing need of configurable plug 'n' play solution which facilitate customer to customize the product their own way. There are a lot of ASSP solution available in the market which are fixable to the board straight away and has removed the hassle of volatile ASIC device which are intended to use for specific application. Considering the requirements, SLS and Altera has come up with a low cost, configurable single chip **MAX10FPGA** solution which allows user to configure multiple IP Cores and provide easy interface to use with any processor with analog and digital signal support. It provides a compact, cost-effective and small-footprint turnkey solution.

This solution includes multiple USB bridge solution on a single chip **MAX10FPGA** device with a flexibility to have single solution as per customer requirement. This application note describes design architecture **MAX10FPGA**, SLS multiple USB bridge solutions using **MAX10FPGA**, its features and advantages.

MAX10FPGA Architecture and Features

Altera's **MAX10FPGA** revolutionizes non-volatile integration by delivering advance processing capabilities in a low-cost, single chip small form factor programmable logic device. Building upon the single chip heritage of previous MAX device families, densities range from 2K-50KLE, using either Single or Dual-core voltage supplies. The **MAX10FPGA** family encompasses both advanced small wafer scale packaging (3mmx3mm) and high I/O pin count packages offerings.

Figure 1. MAX10FPGA Architecture



Dual Configuration Flash

A single, on-die flash memory supports dual configuration, for true fail-safe upgrades with thousands of possible reprogram cycles.

Analog blocks

Integrated analog blocks with ADCs and temperature sensor provide lower latency and reduced board space with more flexible sample-sequencing.

Instant On

MAX10FPGAs can be the first usable device on a system board to control bring-up of other components such as high density FPGAs, ASICs, ASSPs, and Processors.

Nios® II Soft Core Embedded Processor

MAX10FPGAs support the integration of Altera's soft core Nios II embedded processors, providing embedded developers a single-chip, fully configurable, instant-on processor subsystem.

DSP Blocks

As the first non-volatile FPGA with DSP, **MAX10FPGAs** are ideal for high-performance, high-precision applications using integrated 18x18 multipliers.

DDR3 External Memory Interfaces

MAX10FPGAs support DDR3 SDRAM and LPDDR2 interfaces through soft IP memory controllers, optimal for video, data path, and embedded applications.

User Flash

With up to 736 KB of on-die user flash code storage, **MAX10FPGAs** enable advanced single chip Nios II embedded applications. The amount of user flash available depends on configuration options.

SLS USB Solutions using MAX10FPGA

SLS is providing the certified USB solutions from past many years to the clients and they are widely accepted. Considering the face, SLS has approached to a step which can lead the customer direct engage with the IP Core and configure it as per their requirement.

Following is the list of widely used USB solutions requested by customers.

- USB to I2C Bridge
- USB to UART Bridge
- USB to SPI Bridge
- USB Mass Storage using SD Card

Figure 2. USB to UART/I2C/SPI Bridge Architecture

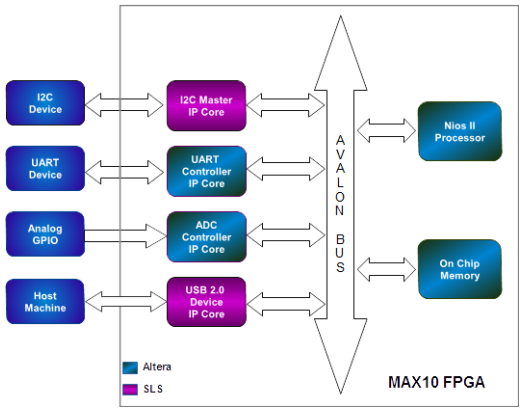


Figure 2. shows block diagram of USB to UART/I2C/SPI Bridge solution which we are going to provide. The block diagram shows **MAX10FPGA** device configured with USB 2.0 Device Controller IP Core to provide USB functionality to the device along with I2C Master Controller, SPI Master Controller and UART Controller IP Core to provide I2C, SPI and UART interface to host machine as per requirement.

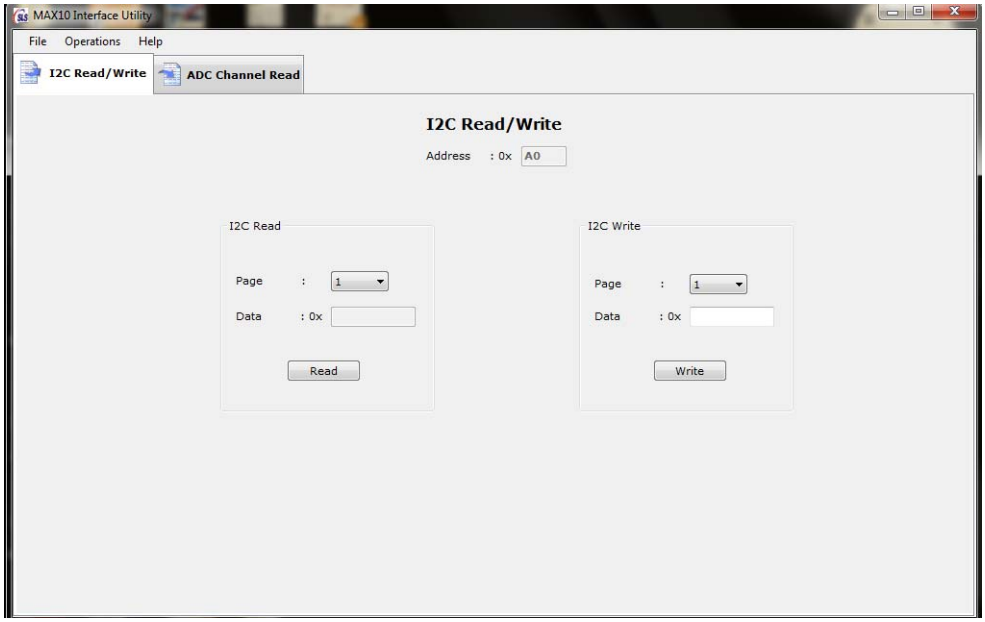
USB to I2C Bridge

Aim of this bridge is to access I2C slave Device using an USB Interface. On the MAX10 Evaluation Kit Add On Board, we have AT24C01C PROM with I2C interface. In order to access this device, SLS has develop a Host application which will read and write the PROM using USB interface. As shown in Figure 2, this design uses the SLS USB 2.0 Device IP Core and I2C master IP

Core to communicate with the I2C Slave device and the Host Machine.

The application will provide the selection of the pages to read/write byte. Figure 3 shows the MAX10 Evaluation Kit Add On Board Interface Utility screen shot.

Figure 3. MAX10 Evaluation Kit Add On Board Interface Utility for I2C Interface



USB to UART Bridge

Aim of this bridge is to provide the UART (RS-232) interface over the USB Interface. The MAX10 Evaluation Kit Add On Board is having a MAX3232 UART (RS-232) Controller for UART interface. As shown in Figure 2, this design uses the SLS USB 2.0 Device IP Core and Altera UART Controller IP Core to implement the USB to UART bridge. On successful enumeration of the USB device, it appears as a COM Port in the Host machine. This allows a user to access the UART port over USB.

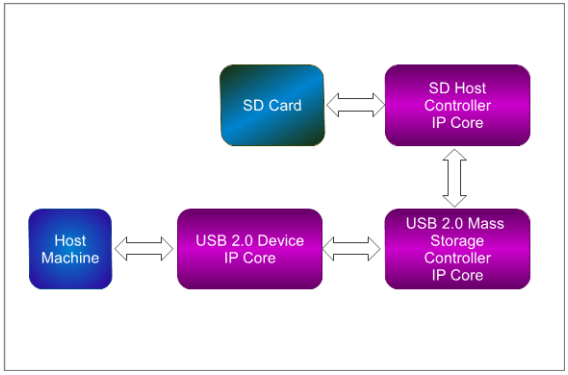
To test the interface, use the TeraTerm or RealTerm Host applications, make settings and open the COM port. Short the Tx and Rx pins on the DB9 connector of the board. This allows user to perform a loop- back test. Type

any character in the Host application and the same character will be received in the application.

USB Mass Storage using SD Card

Aim of this bridge is to provide the external USB Mass storage device. The MAX10 Evaluation Kit Add On Board is having a SD Card interface to implement the mass storage bridge. As shown in Figure 4, this design uses SLS USB 2.0 Device IP Core and SLS SD Host Controller IP Core to implement the USB mass storage solution. On successfully enumeration of the device, it appears as a new drive in the Host machine. This allows to read/write the data to/from the SD card using the USB interface.

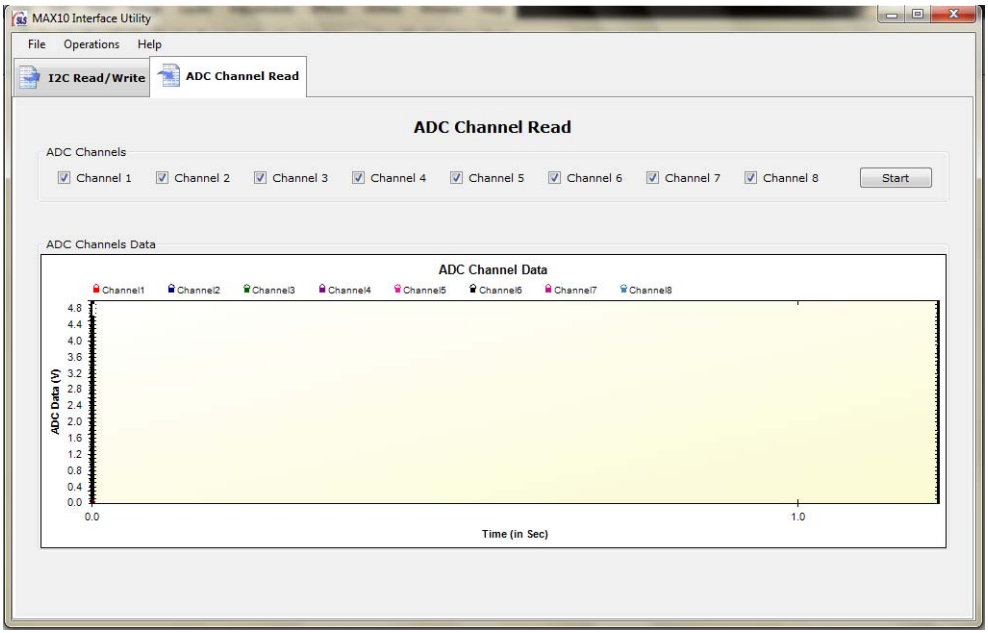
Figure 4. USB Mass Storage using SD Card Architecture



USB based ADC Interface

Aim of this design is to provide the ADC interface over USB interface. The MAX10 Evaluation Kit Add On Board is having Analog GPIO headers which is directly connected to Altera MAX10 FPGA. As shown in Figure 2, this design uses the SLS USB 2.0 Device IP Core and Altera's ADC interface IP Core. On successful enumeration, the MAX10 Evaluation Kit Add On Board interface utility provides the option to select ADC channels to display the analog input signals. Figure 5 shows the screen shot of the MAX10 Evaluation Kit Add On Board interface utility for ADC interface.

Figure 5. MAX10 Evaluation Kit Add On Board Interface Utility for ADC Interface



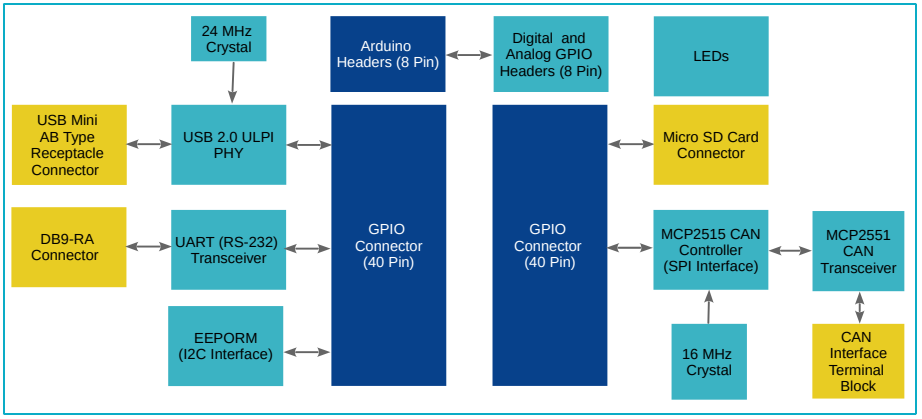
Features of SLS USB Solutions

- Easy to Use
- Plug and Play
- Configurable
- Compact
- Low Scale
- Robust and Reliable

Evaluation Platform

The Altera has developed the **MAX10FPGA** evaluation kit for evaluation. SLS is going to develop the Add on board which can be snapped on the **MAX10FPGA** evaluation kit and provides all the interface for on a single board. Following is the block diagram of the Add on board. It provides interface for SPI, I2C, UART and SD card devices which makes the development faster and easier.

Figure 6. MAX10 Evaluation Kit Add On Board



Advantages

- Easy to interface with any processor.
- Compatible with most operating systems.
- Programmable as per the requirement.
- Cost effective pricing.
- Provide evaluation platform which makes the development easier.

Further Information

Download application for MAX10 Evaluation Kit Add On Board Interface Utility for I2C and ADC interface from http://www.slscorp.com/downloads/add-on-board-pkgs.html

Download reference design for MAX10 Evaluation Kit Add On Board from http://www.slscorp.com/downloads/add-on-board-pkgs.html

For more information about SLS USB solutions, write us at info@slscorp.com.

Revision History

Table below shows the revision history of this application note.

Version	Date	Description
1.1	March 2015	Added USB to I2C Bridge, Reading Internal ADC, USB to UART Bridge
1.0	January 2015	First Release of the Application Note

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